Efficiency Improvement of Differential Drive Rectifier for Wireless Power Transfer Applications

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Abstract — In this paper, the power conversion efficiency of a 0.18 μm CMOS differential drive (DDR) full-wave rectifier was improved by optimization technique of the rectifier. The optimized rectifier achieves 83.3 % power conversion efficiency (PCE) at -16.3 dBm input power, with an input RF of 953 MHz and 0.6 V peak sinusoidal signal. The voltage conversion ratio becomes 72.3 % at -13 dBm input power. The output average voltage equals 0.4 V at peak input voltage 0.6 V, whereas the conventional DDR rectifier achieves PCE = 75.4 % at an RF input power Pin = -12.5 dBm and output average voltage of 0.15 V at the same peak input voltage. The optimized rectifier is suitable for such applications that require minimum RF input power as UHF RFID tag and implantable medical devices (IMDs).

Keywords — CMOS differential drive, rectifier, power conversion efficiency, voltage conversion ratio, implantable medical devices

I. INTRODUCTION

There has been a considerable interest in the development of wireless power transfer systems, since their applications are numerous and varied such as implantable medical devices (IMDs) [1], [2], wireless sensor networks and RFID devices [3], [4], [5]. RF energy harvesting is one of the well known methods of wireless power extraction [4]. Fig. 1 shows a simple model of RF energy harvesting system [6]. The main block of energy harvester is the rectifier as it converts the ambient radio frequency (RF) power to direct current (dc). Recent studies of RF to DC rectifier are focused on many issues among them improvement of both power conversion efficiency (PCE) and voltage conversion ratio (VCR) with acceptable minimum input power [7], [8], [9]. The PCE of a CMOS rectifier can be improved by increasing the MOS transistors size (W/L) [10], which in turn reduces the equivalent input impedance of the rectifier and decreases the charging time of load capacitor, hence the speed of switching action will be raised [9]. There are different configurations for the conventional rectifier circuits. The basic rectifier architecture is based on Schottky diode [11] with a small barrier voltage of 0.2V to 0.3V. This type of rectifier exhibits large DC output voltage. But its manufacturing cost is very expensive, and it is not available in standard CMOS process [5]. Diode-connected load CMOS transistors are used to mimic the role of Schottky diode in rectifier circuits [12]. The DC output voltage is produced by subtracting the CMOS transistors threshold voltages from the low input voltage which limits the PCE. To address this issue, Kotani et. al., introduced a rectifier called self-Vth-cancellation (SVC) [13], [14]. In this technique, the gate-source voltage of NMOS and PMOS are provided by the DC output voltage. It has cons that there is no way to control the voltage at the gates of the MOS devices. Once the output amplitude exceeds threshold voltage of the devices, they turn on at the same time causing very high leakage currents. The SVC rectifier was designed and fabricated in 0.35μm CMOS 2P3M technology [13], [14] and exhibited a peak PCE of 32% at -10dBm of input power. A new CMOS full wave rectifier designated for IMDs was developed by [15]. It uses bootstrapped capacitors to reduce the effective threshold voltage of selected MOS switches. This rectifier achieved higher power efficiency over a wide range of input peak amplitude higher than 0.8V. But this range of input voltages is very large compared to requirements of micro-power applications. Besides, the author neglected the body effects of MOS devices resulting from different bulk biasing. A cross-connected differential drive rectifier (DDR) accomplished power conversion efficiency PCE of 67.5% at an RF input power -12.5dBm in TSMC 0.18μm CMOS process [11], [12]. The peak output voltage of the DDR circuit is obtained by subtracting the drain to source voltage of MOS transistor from input voltage amplitude instead of threshold voltage. The pros and cons of those different RF to DC rectifier topologies were presented, compared and designed in a 65 nm CMOS process [4]. The differential drive (DDR) topology has the best maximum PCE. It was about 65% while the SVC technique was 46.7% and the MOS diode topology was 51%. It is obvious that the required range of RF input power for turning on the rectifier varies according to the application that uses this power. The maximum RF input power limitation of medical devices decided to 25μwatt (-16dBm) [16]. The tag power of RFID generally varies from 10μW (-20dBm) to 100μW (-10dBm) [17]. Accordingly, the DDR configuration was optimized for an RF input power range from -20dBm to -10dBm. The scope of this study is to improve both PCE and VCR of the conventional DDR and to lower its RF input power to be suitable for applications as implantable medical devices IMDs and RFID devices. To achieve those goals; an optimization procedure by Agilent ADS (Advanced Design system) software has been used. In this paper two rectifying circuits are presented, the conventional DDR circuit [17] and the original one with a modified circuit parameters. The paper is organized as follows: The conventional DDR basic principle...
and its simulated results are provided in section II. Section III shows the simulation results of optimization of the rectifier. Finally conclusion is represented in section IV.

II. STUDYING CONVENTIONAL DDR CIRCUIT

A. Rectifier Basic Operation

The conventional DDR circuit is shown in Fig.2. It has differential input voltage as in (1). The differential input voltage is applied across two points Vina and Vinb. It has amplitude (Vmax) and frequency (Fre) as seen in (2) [9]. The circuit consists of four transistors, two PMOS-devices (Mp1, Mp2) and two NMOS transistors (Mn1, Mn2). At positive half cycle of input voltage signal, when Vmax > 0, both Mp1 and Mn2 turn on as soon as Vmax reaches the threshold voltages of those devices. At the same time transistors Mp2 and Mn1 operate into sub-threshold region. The pulsating DC output voltage is given by subtracting the drain to source voltages of both Mn2 and Mp1 from the peak input voltage, and vice versa for negative half cycle.

\[ V_{\text{out}} = V_{\text{peak}} - (2 \times V_{\text{th}}) \]  

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B. Simulation Results of Conventional DDR

The DDR circuit is simulated by the ADS software. The input current and the voltage waveforms of internal RF nodes (Vx, Vy) and output voltage are shown in Fig.3. The PCE of a rectifier is controlled by several parameters such as circuit topology, input signal voltage (frequency, amplitude) CMOS device parameters (width, length), and circuit components values such as coupling capacitors, output load resistor and load capacitor. Therefore, the dependence of the PCE of the DDR rectifier on parameters was extracted using simulation as shown in Fig.4. Fig.4b shows the inverse relation between the PCE and the input signal frequency. It is seen from Fig.4c that the PCE can be increased by getting higher load resistor. The VCR is defined as the ratio of the average output voltage to the peak input voltage. Both the voltage conversion ratio VCR and the output average voltage of the conventional DDR are drawn in Fig.5.
The proposed DDR in [17] is optimized and simulated in TSMC 0.18µm technology using ADS software. The values of circuit parameters of both conventional DDR and optimized DDR are presented in Table I. Performance comparison between the conventional DDR and the optimized DDR is shown in Table II. The input current and the output voltage waveforms are shown in Fig. 6. The reliance of PCE on different parameters is shown in Fig. 7. The voltage conversion ratio and the average output voltage are also improved to higher value at lower RF input power as described in Fig. 8.

III. SIMULATION RESULTS OF OPTIMIZED RECTIFIER

Table I. Values of Circuit Parameters of the Conventional and the Optimized DDR

<table>
<thead>
<tr>
<th>Circuit Parameters</th>
<th>Vmax (V)</th>
<th>Fre (MHz)</th>
<th>Wp (µm)</th>
<th>Wn (µm)</th>
<th>Ccoup1 (pf)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional DDR</td>
<td>0.92</td>
<td>953</td>
<td>18</td>
<td>3.6</td>
<td>1.13</td>
</tr>
<tr>
<td>Optimized DDR</td>
<td>0.6</td>
<td>953</td>
<td>472</td>
<td>83.618</td>
<td>5.77</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Circuit Parameters</th>
<th>L (µm)</th>
<th>Rload (KOhm)</th>
<th>CL (pF)</th>
<th>Ccoup2 (pf)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional DDR</td>
<td>0.18</td>
<td>10</td>
<td>1.13</td>
<td>1.13</td>
</tr>
<tr>
<td>Optimized DDR</td>
<td>0.18</td>
<td>10</td>
<td>1.13</td>
<td>42</td>
</tr>
</tbody>
</table>

Table II. Performance Comparison between the Conventional DDR and the Optimized DDR

<table>
<thead>
<tr>
<th>Simulation Result</th>
<th>Steady State Time (nsec)</th>
<th>Iin (peak) (mA) @ Vmax (V)</th>
<th>Vout (mV) @ Vmax (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional DDR</td>
<td>14</td>
<td>0.291 @ 0.92</td>
<td>658 @ 0.92</td>
</tr>
<tr>
<td>Optimized DDR</td>
<td>7</td>
<td>2.598 @ 0.6</td>
<td>447 @ 0.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulation Result</th>
<th>PCE (%) @ Pin (dBm)</th>
<th>VCR (%) @ Pin (dBm)</th>
<th>Vout_avg (mV) @ Vmax (V)</th>
<th>Zin (Ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional DDR</td>
<td>75.39 @ -12.5</td>
<td>71.85 @ -10.48</td>
<td>157 @ 0.6</td>
<td>103</td>
</tr>
<tr>
<td>Optimized DDR</td>
<td>83.34 @ -16.37</td>
<td>72.297 @ -13.08</td>
<td>439 @ 0.6</td>
<td>4.45</td>
</tr>
</tbody>
</table>
This paper presented an optimization technique to improve the rectifier PCE. The circuit was simulated using TSMC 0.18 μm CMOS technology. It was found that the rectifier PCE depends on many parameters such as transistor size, coupling capacitors, and input signal frequency. The optimized circuit shows that the PCE has increased to 83.3% at -16 dBm input power. The VCR reaches 72% at Pin = -13 dBm and the output average voltage equals 0.4 V at a peak input voltage of 0.6 V whereas the conventional DDR rectifier gives PCE = 75% at RF input power Pin = -12.5 dBm and the output average voltage equals 0.15 V at the same peak input voltage. The input impedance magnitude changes from 103 Ohm to 4.4 Ohm at an input power Pin = -16 dBm. Therefore, the optimized rectifier is suitable for such applications that require minimum RF input power as UHF RFID tag and implantable medical devices (IMDs).

REFERENCES


