Design of 0.35 μm CMOS Temperature Sensor for Automatic Refresh Cycle in DRAM Memory Cell

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Abstract—This paper proposes a low power CMOS smart temperature sensor which is composed of temperature-to-pulse generator (TPG), time-to-digital converter (TDC), and frequency selector. The multiple-block system is to obtain the self-refresh operation for a low power memory cell. Temperature-to-pulse generator (TPG) is composed with two delay-lines which are obtained by the circuit of CMOS inverter. The propagation delay time of CMOS inverter has a dependency on temperature. The inverter-based delay line and feedback topology are applied in TDC. The small-size time-mode temperature sensor is designed with 0.35-μm CMOS process. Six different digital outputs are obtained for the temperature ranges of -40 ~ 100 °C. Simulation test shows that the proposed temperature sensor is operated with the low power dissipation of 0.075 μW per sample and die-area of 0.06 mm².

Keywords—Temperature sensor; TPG; TDC; Self-refresh; Frequency selector

I. INTRODUCTION

Dynamic random-access memory (DRAM) chip which is widely used in computer or communication systems consists of the cells in which the bits are stored. Each memory cell in DRAM is an electronic circuit capable of storing a bit in a capacitor. Among the various DRAM operations, refresh operation on bit lines takes major portion to decide the DRAM frequency and its leakage current. A periodic refreshing is to regenerate the data stored on capacitors in memory cells. As the memory size of DRAM increases and its operating voltage decreases, refresh operation is difficult to meet the design requirements of power consumption and speed. Method of self-refresh control is proposed in the smart temperature sensor in order to improve the memory performance [1-4].

In this work, high performance refresh control is obtained by temperature sensor and time-to-digital converter (TDC) [5-7] which are being widely used for thermal and time-interval management system. Conventionally, a certain temperature in sensor can be changed into a pulse duration, which provides digital signals by TDC. The important issue of the sensor is low power dissipation and its accuracy. In order to obtain time-variant refresh operation and low power consumption in memory cell, we propose a digital refresh control circuit which has a short refresh period in the range of milli-seconds (ms) which can covers the operation temperature range of -40 ~ 100 °C.

In MOS transistor, the effect of temperature on carrier mobility and threshold voltage are well known [8-10]. Temperature is supposed to be proportional to the propagation delay which depends mostly on the mobility. As the temperature increases, the mobility in MOS transistor decreases [1] and drain current is linearly proportional to the mobility. In time-domain temperature sensor, the on-off switching delay times of CMOS inverter circuit is crucial to decide the temperature resolution and the accuracy of time measurement conversion.

Smart temperature sensor in this work is the following steps. First, temperature is changed to be the pulse of the delay times, then, the pulse time is represented as the digital signal, finally, the digital signal provides a proper frequency for the refresh operation in DRAM memory cell.

II. CIRCUIT DESCRIPTION

The block diagram of self-refresh controller is shown in Fig. 1, which has temperature-to-pulse generator (TPG), time-to-digital converter (TDC), and frequency selector.

A. Temperature-to-Pulse Generator

Fig. 2 (a) is the temperature-to-pulse generator (TPG) which is composed with two delay-lines and exclusive OR gate. The pulse-difference between two delay-lines is the output of TPG. CMOS inverter shown in Fig. 2 (b) is used to obtain a delay-time which depends on the aspect ratio (W/L) which is the ratio of MOS channel width and length. As mentioned before, propagation delay time depends on the mobility and threshold voltage. As the effect of temperature variation on MOS threshold voltage is small, the propagation delay time of CMOS inverter depends mostly on the variation of the mobility. Mobility is inversely proportional to the temperature and the delay time has a linear dependence on the inverse of mobility, hence, the delay time has a property of PTAT (proportional to absolute temperature) [2]. With increase of temperature, the mobility decreases, hence, the delay-time which is the propagation
delay of CMOS inverter is supposed to increase. In CMOS
inverter, thermal compensation circuit which has the diode-
connected MOSFETs can be included to reduce the thermal
sensitivity of current.

\[ \text{Delay Line (200ns)} \]

\[ \text{Delay Line (100ns)} \]

\[ \text{Low Thermal Sensitivity} \]

B. Time-to-Digital Converter

Two types of smart temperature sensor are known to be
electric-domain and time-domain. The time-domain smart
temperature sensor has an advantage of simplicity of circuit
design and small die-area, although the voltage-domain
sensor is known to have extremely high accuracy. Time-to-
digital converter (TDC) is a key element in time-domain
smart temperature sensor and generally uses a cyclic delay
line. Fig. 3 (a) is the block diagram of TDC, where the
circuits of pulse-shrink and delay and digital 5 bit counter are
included with feedback circuit [11]. The output of pulse-
shrink circuit determines the digital output by the numbers of
the high or low clock pulse. The feedback path continues to
activate until the final digital output is obtained, and the
pulses of P-SRK-OUT in Fig. 3 (a) is in the high logic state
after every 200 ns of time delay. The circuit of pulse-shrink
is shown in Fig. 3 (b). Two CMOS inverters are the buffer
which produces a switching delay time.

\[ \text{Feedback Path} \]

\[ \text{Pulse_shrink} \]

\[ \text{Delay 200n} \]

\[ \text{5Bit Counter} \]

C. Frequency Selector

The schematic of frequency selector which is composed
of 3-bit decoder, oscillator, and frequency divider [12] is
shown in Fig. 4 (a). Oscillator provides the clock pulse, and
frequency divider which is composed of 6 flip-flops for the 6
different temperature ranges provides the 6 variable
frequencies. D flip-flops are used as the frequency divider,
and the operating frequency is low under MHz range. The 5-
bit digital output in TDC is changed into the 3-bit signal
output, and, then, the 3-bit signal is changed into the 6 output
signals through the decoder. Multiplexer of Fig. 4 (b) selects
a refresh clock pulse among the 6 output signals of decoder.
The component of multiplexer is the transmission gate.
III. RESULT

Pulse width and characteristic of temperature-to-pulse generator (TPG) are shown in Fig. 5 (a) and (b). Pulse width is determined from the difference between the two delay lines in TPG. Temperature sensitivity is 0.86 ns/°C. The temperature range can be determined by the number of delay cells in delay line. The reduction in the number of delay cells causes the extension into more negative temperature range.

The operation of the proposed self-refresh controller is shown in Fig. 6, where the output signals (SRF-OUT) of 85.3 and 2.6 ms are obtained at the input temperatures of -40 and 100°C respectively. The START signal triggers the refresh controller for the period of 50 μs, which is an enough sensing time for the operation of TDC block. The pulse-shrink output (SK-OUT) in TDC block provides a shorter period time when START signal comes to end. At the end of the START signal, a proper digital signal is activated and the output signal is finally obtained. The period of output signal decreases with increase of the temperature. Advantage of the proposed TDC is the simple system block which is composed of pulse-shrink circuit and counter, therefore, low power dissipation is expected. In this pulse-shrink circuit which is composed of CMOS inverter logic circuit, another element to decide a delay time is the device parameter of MOS transistor. One of parameter to obtain a proper delay time in this work is the duty ratio of the channel width versus length (W/L). Threshold voltage in MOS can be another parameter, but it has a nonlinear relationship with the delay time, furthermore, its thermal coefficient is quite small to obtain a variable delay time.

The signals of pulse-shrink output with 6 different temperatures are shown in Fig. 7, where the digital outputs of 000, 010, 011, 100, 101, and 110 are also shown at the temperatures of -40, 10, 10, 50, 80, and 100°C respectively. In the signals of pulse-shrink output, the lower temperature provides a smaller number of clock pulse. The variation of pulse width in TPG is shown in Fig. 5, where the pulse width indicates a linear dependence on temperature. The pulse width affects the numbers of clock pulse shown in Fig. 7. The Feedback topology in TDC causes the dependence of settling time on the pulse width. The settling time shows to be almost linearly proportional to the numbers of clock pulse. Self-refresh clock-pulse for a memory cell is shown in Fig. 8. Self-refresh period at room temperature of 30°C is 21.3 ms. Table I is the summary of the self-refresh period with 6 different temperature-ranges. The refresh frequency in the temperature-range of 5 ~ 35°C is 46.8 Hz. In the lower temperature of -30 ~ 5°C, the frequency is designed to be 23.4 Hz. Power consumption per sample in this proposed temperature sensor is 0.075 μW with die-area of 0.06 mm². Discussion in terms of temperature-range, resolution, and accuracy is in a lower concern in this work because temperature sensor mostly consists of digital circuits and specification depends on the design parameters of circuit. Our emphasis is a small die-area due to the simple circuitry which provides low power dissipation and cost.
Figure 8. Self-refresh clock-pulse for a memory cell at the 3 different temperatures.

<table>
<thead>
<tr>
<th>Temp.(°C)</th>
<th>Logic output</th>
<th>Freq. (Hz)</th>
<th>Period (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40 ~ -30</td>
<td>001</td>
<td>11.7</td>
<td>85.3</td>
</tr>
<tr>
<td>-30 ~ -5</td>
<td>010</td>
<td>23.4</td>
<td>42.6</td>
</tr>
<tr>
<td>-5 ~ 35</td>
<td>011</td>
<td>46.8</td>
<td>21.3</td>
</tr>
<tr>
<td>35 ~ 65</td>
<td>100</td>
<td>93.7</td>
<td>10.6</td>
</tr>
<tr>
<td>65 ~ 95</td>
<td>101</td>
<td>187.5</td>
<td>5.3</td>
</tr>
<tr>
<td>95 ~ 100</td>
<td>110</td>
<td>375.0</td>
<td>2.6</td>
</tr>
</tbody>
</table>

TABLE I. SELF-REFRESH PERIOD WITH CHANGE OF TEMPERATURE

IV. CONCLUSION

In this paper, CMOS smart temperature sensor is proposed for an automatic refresh controller in DRAM memory cell. The time-domain temperature sensor which has an advantage of low power dissipation and small die area is composed of temperature-to-pulse generator (TPG), time-to-digital converter (TDC), and frequency selector. The function of pulse and time measurement is performed by the delay time caused by CMOS inverter. Simulation study in 0.35-μm CMOS process shows that the proposed sensor achieves a six digital output in the temperature range of -40 ~ 100 °C with power dissipation of 0.075 μW, resolution of 0.5 °C, and die-area of 0.06 mm². This feature demonstrates that the proposed temperature sensor is an excellent low power refresh controller for a mobile DRAM memory cell.

REFERENCES