Low Power CMOS 8:1 Injection-Locked Frequency Divider with LC Cross-Coupled Oscillator

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Abstract—This paper proposes a high performance frequency divider which is composed of injection-locked frequency divider (ILFD) and current-mode logic (CML) frequency divider. The multiple-block divider is to obtain the broad-band and high frequency operation in phase-locked loop (PLL). ILFD has a similar structure with LC cross-coupled oscillator which operates at 20 GHz. 3 stages of ILFD are supposed to provide the operation of divide-by-8 (/8) with low power consumption and are to adjust the frequency alignment with the LC cross-coupled oscillator. CML frequency divider which is used as the 2nd block of divider applies an inductive peaking structure in order to increase the bandwidth. The proposed frequency divider which has the /8 ILFD and /32 CML frequency divider is integrated with 0.18 µm CMOS process and operates in the conventional PLL. Simulation test shows the low power consumption of 13.2 mW at the input frequency of 20 GHz.

Keywords—Frequency divider; ILFD; CML; PLL; CMOS

I. INTRODUCTION

PLL is used in many communication systems such as clock generation circuit and frequency synthesizers. A frequency divider [1-4] is one of the important elements in PLL system [5-6] which is typically composed of phase detector, charge-pump [7], filter, VCO (voltage-controlled oscillator), and frequency divider. The generation of high frequency and low power consumption are mostly dependent on VCO and frequency divider. The first step of frequency oscillation is in VCO which can be controlled by an input voltage. Recently, several frequency dividers such as super-dynamic, injection-locked, and CML divider are introduced for the advantages such as high-frequency operation, low power consumption, and wide locking range. These important issues are also the critical design parameters of the VCO. CML frequency divider is widely used in a conventional PLL because of a wide frequency range, but its power consumption increases significantly with increase of the operating frequency. ILFD [8-10] is reported to operate in high frequency with low power consumption. However, it has a narrow locking range and suffers from large power consumption with increase of the division ratio.

In this work, injection-locked and CML dividers are applied as the first and 2nd blocks of the divider chain for low power consumption with high-frequency operation. The structure of ILFD is taken similar to that of VCO for a better frequency alignment. LC cross-coupled oscillator is used as-VCO for high-frequency operation. 3 stages of ILFD are used in this work for low power consumption in 1/8 frequency division. CML divider which is the 2nd block is composed of the master-slave flip-flop, and has an inductive peaking structure with DC bias for a current source. The frequency divider is designed with /8 ILFD and /32 CML divider in 0.18-µm CMOS process. The divider is applied in the conventional analog PLL and electrical measurement is done by the CADENCE simulation.

II. CIRCUIT DESIGN OF DIVIDER

VCO and ILFD are shown in Fig. 1 (a) and (b), respectively. VCO has the cross-coupled n- and p-MOSFETs. Operating frequency of VCO depends on the passive parameters inside the circuit. A specific capacitance can be obtained by the control voltage $V_c$ which is applied in the drain-sources in the n-channel MOSFETs $M_{N1}$ and $M_{N2}$.

ILFD uses a CMOS oscillator with a complement structure. Injection is driven by the input signals through the gates of the MOSFETs $M_{P3}$ and $M_{P4}$. MOSFETs $M_{P1}$ and $M_{P2}$ are the cross-coupled p-MOS pair, while a complement topology is obtained by the n-MOSFETs $M_{N1}$ and $M_{N2}$. The MOSFETs resemble the differential pairs whose output is fed back to its input. In the locking state, the zero crossings of $V_{out}$ and its reverse coincide with the peaks of the input signals. The differential operation provides a division ratio of...
2. The operating frequency is determined by the inductance of the inductor and the parasitic capacitance of MOSFETs. The block diagram of PLL is shown in Fig. 2, which has a 20 GHz LC VCO, 1/8 ILFD chain, and a 5-stage CML frequency divider. The input of ILFD is the fundamental signal \( f_{\text{in}} \) which is the output frequency of VCO. In this work, 3 ILFD’s are designed for 1/8 frequency division. CML frequency divider is applied for a 32 division ratio which is obtained from the 5-stage flip-flops. PLL also includes the phase frequency detector (PFD) and charge pump (CP). The output of the CML divider is another input frequency of PFD which is about 100 MHz which comes from ILFD (1/8) and CML (1/32) dividers at the VCO output of 20 GHz.

![Figure 2. Block diagram of PLL with ILFD and CML frequency divider.](image)

In PLL, the operation of frequency divider is to reduce the output frequency of VCO to that of the reference clock. Fig. 3 is the CML frequency divider [2] which is composed with two level-sensitive CML master-slave flip-flop. The master-slave flip-flop which can be commonly constructed in integrated circuit form operates as the read and latch circuits. The read circuit is the n-MOS differential pair and the latch circuit is the cross-coupled MOSFETs in the block. The state change of the master and slave takes place on the rising and the next falling edges of the clock pulse. The change occurs regardless of pulse width. Therefore, as long as the clock pulse width exceeds a certain minimum value, proper operation of the latch does not depend on pulse width and the error due to the rising and falling times can be protected.

![Figure 3. Schematic of CML frequency divider.](image)

CML divider with an inductive peaking structure is designed to provide a 1/32 frequency division with a 5-stage chain. The DC bias in MOS gate is applied in the frequency divider in order to improve a current driving capability and ensure the MOSFETs to act in the forward-active region. The block diagram of the odd and even CML dividers is shown in Fig. 4, where D flip-flops, clock pulse (CLK), and control signal (\( C_{\text{cont}} \)) are included with the OR and AND gates. The odd and even dividers are the 3:1 and 2:1 static divider respectively. The even (odd) clock frequency is obtained when the control signal is high (low).

![Figure 4. Block diagram of the odd(3) and even (2) divider.](image)

### III. RESULT

The output waveforms of ILFD and CML frequency dividers are shown in Fig. 5 which is obtained by the simulation of CADENCE Spectre. Fig. 5 (a) is the input (A) and output (B, C) waveforms of the ILFD. The waveforms of 10 (B) and 5 (C) GHz are the outputs of the 1st and 2nd ILFDs respectively. The 20 GHz input frequency is shown in (A) which can be obtained from VCO. ILFD has an advantage of high frequency operation with relatively low power consumption, although it has a narrow locking range.

![Figure 5. (a) output waveforms (B, C) of the 1st and 2nd ILFDs with 20 GHz input frequency (A), (b) output waveforms (a, b) of 160 and 80 MHz of CML divider.](image)
On the contrary, CML frequency divider which is applied after 3 ILFDs can operate at wide bandwidth. However, its power consumption significantly increases with increase of the operating frequency. Fig. 5 (b) is the output waveforms of the 2 CML dividers, whose frequencies are 160 and 80 MHz respectively. The operation of divide-by-2 is perfectly obtained, and the waveforms look to be a clock-pulse, while the output waveform of ILFD looks to be a sinusoidal wave. Because CML divider operates as a digital logic circuit which is a master-slave flip-flop, the output waveform looks more to be a clock pulse rather than a sinusoidal wave.

Fig. 6 is the block diagram of the divider and the output waveforms. The block diagram of divider in Fig. 6 (a) has a 3-stages ILFD and a 5-stages of CML divider. Fig. 6 (b) is the output waveforms with 8 stages of even divider at the input frequency of 20 GHz.

The simulation is obtained from the post-layout simulation of 0.18 µm CMOS process. The outputs of each divider show the exact signals which are divided by 2 of the input signals. The final output \( \overline{\text{I}} \) in Fig. 6 (b) shows the frequency of 80 MHz which is an approximate period time of 13 ns. The final output \( \overline{\text{I}} \) is obtained after the 8-stages frequency dividers as mentioned in Fig. 6 (a). The 32:1 CML dividers show the proper operation of the 2-dividend at each stages from \( \overline{\text{E}} \) to \( \overline{\text{I}} \). The power consumption of ILFD is about 1.2 mW with the supply voltage of 1.2 V and the frequency of 10 GHz. Total power consumption of the 8-stages frequency dividers is 13.2 mW, while the 3 ILFDs consumes approximately 4.5 mW. With decrease of the operating frequency, the power consumption of divider also decreases. The CML divider is found to consume a more power. Compared to the circuit of ILFD shown in Fig. 1(b), the circuit of CML divider in Fig. 3 has a more switching MOS devices which cause a more power consumption. Many other researches usually use a single ILFD for the frequency divider in PLL, while this work implies three stages of ILFD. Under 50 GHz frequency locking in PLL, single-stage ILFD is a sufficient frequency divider for the locking of VCO output, however, this work is concerned in a low power consumption with large number of division ratio. The number of MOS switches inside ILFD is much smaller than that of CML divider, therefore, the power consumption can be significantly reduced by the application of ILFD.

In the final stage of the divider of Fig. 6 (a), an output buffer is applied to create enough output voltage swing. It can also provide a more stable output, although it cost a larger power consumption or die-area. Fig. 7(a) shows the circuit of buffer which consists of a differential pair and a current mirror. Fig. 7 (b) is the output waveforms when the CML divider incorporates with and without buffer. The waveform (B) which is obtained with buffer indicates that buffer provides a more stable waveform with larger swing. It is obtained at the input of 20 GHz with the proposed 2:1 CML divider. The main concern for VCO design is high frequency capability and wide locking range with low power consumption. The VCO in this work adopts LC cross-coupled topology. LC oscillators are difficult to tune over wide range, while crystal oscillator operates at a single frequency. Fig. 8 shows the characteristic of output frequency with change of the control voltage of \( V_c \). The range of linearity region in \( f_{out} \) is from 14 GHz to 26 GHz, and the output frequency of 20GHz is obtained at the control voltage of 0.6 V.
As mentioned in Fig. 1 (a), the gates in the MOSFETs of M_{N1} and M_{N2} provide the capacitance with variation of the control voltage V_c. Fig. 8 shows the narrow range of the linearity region which is about 1.2 V in the control voltage. To increase the linearity region of f_{out} is a major concern in VCO. To increase the linearity region in the characteristics of frequency-voltage gain, varactor requires to be in parallel with the MOSFETs of M_{N1} And M_{N2} in the VCO.

The output frequency spectrum of VCO and ILFDs is shown in Fig 9, which is obtained from the post-layout simulation. Three high power peaks of α, β, and γ are shown at the frequencies of 20, 10, and 5 GHz, which are the operation results of VCO, 1st ILFD, and 2nd ILFD. The result indicates that the divide-by-two operation by ILFD is done accurately and VCO produces the high frequency of 20 GHz by the gate capacitance in MOSFET.

### IV. Conclusion

In this paper, multiple-stages of injection-locked frequency divider (ILFD) are applied in PLL in order to obtain a high frequency operation with low power consumption. 3-stages ILFD and 5-stages CML divider are to obtain the 1/8 and 1/32 frequency divisions at the input frequency of 20 GHz. The ILFD has a LC cross-coupled topology which is also applied to VCO, while CML divider applies an inductive peaking structure in the master-slave flip-flop. Simulation study in 0.18-µm CMOS process shows that the proposed divider operates accurately to provide an approximately 80 MHz divided-frequency which is required for the input of PDF in PLL. At the supply voltage of 1.2 V, the power consumption of single ILFD and total 8 dividers are about 1.2 mW and 13.2 mW, respectively.

### REFERENCES


