Advances in High-Speed Real-Time Simulation

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Why Real-Time?
Simulation running at true speed allows connection to real hardware
Hardware can be tested in absence of real system
Plant operators, pilots etc. can be trained under realistic conditions

Why High-Speed?
For many systems frame times can be tens of milliseconds or longer
Systems with fast dynamics or rapid switching need shorter frames
Power electronic systems may need microsecond frame times

Acknowledgements
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Team Members
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Initial Research Goals
• Traditional power-system simulation used 50-µS frames
• Modern power-electronic systems involve rapid switching
• Accurate simulation of these systems needs shorter frames
• Initial target was 10-µS frame time for typical systems (later reduced to 2-µS)
• Off-the-shelf, low-cost components – no custom hardware
Choice of Technology

- Many real-time simulations use a real-time version of Linux running on a high-performance PC
- Operating system jitter (of the order of 10 µs) limits minimum frame time
- Higher-performance is possible from systems with Pentium or PowerPC based processors but only with custom designs
- Initial solution: arrays of digital signal processors inserted in PCI bus of conventional PC with Windows OS running on host – no problems with OS jitter, off-the-shelf components.

DSP Issues

- Scheduling Processor Tasks
  - Equalizing processor execution times
  - Minimise inter-processor data transfers
- Internal Data Transfer
  - Common memory vs. link ports
- External Data Transfer
  - Digital and analog outputs and inputs
- Code efficiency
  - Hand-coding vs compiler efficiency
  - Identify efficient HLL code sequences
Software Issues

- Choice of numerical integration algorithm
  - Euler vs Runge-Kutta vs implicit trapezoidal vs state-transition methods
  - Analyse and monitor accuracy and stability of numerical integration
  - Combine differential equations with integration algorithm before coding
  - Minimize total mathematical operations

- Hand coding vs optimizing compiler
  - Hand coding may be needed if compiler can’t exploit processor architecture
  - Use HLL constructs that produce more efficient code

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DSP Performance

<table>
<thead>
<tr>
<th>Model/Platform</th>
<th>Minimum Frame Time</th>
<th>Processor</th>
<th>Clock Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 Pulse BTB - Hammerhead Board, 23 ODEs</td>
<td>16 µs</td>
<td>AD 21160 DSP</td>
<td>80MHz</td>
</tr>
<tr>
<td>6 Pulse BTB - TigerSharc Board, 23 ODEs</td>
<td>3.88µs</td>
<td>AD TS101 DSP</td>
<td>256MHz</td>
</tr>
<tr>
<td>12 Pulse BTB - TigerSharc Board, 39 ODEs</td>
<td>4.5µs</td>
<td>AD TS201 DSP</td>
<td>500MHz</td>
</tr>
<tr>
<td>6 Pulse BTB - TigerSharc Board, 23 ODEs</td>
<td>2.02µs</td>
<td>AD TS201 DSP</td>
<td>500MHz</td>
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Graphical Output

Watch this space
The Need for Multi-Rate Real-Time Simulation

- CSU, Chico developed HSRT simulations with frame rates up to 500 KHz (2-µS frame times)
- These frame rates are needed for power electronic components but not for slower system components such as motors, mechanical components, thermal effects etc.
- Multi-rate real-time simulations simulate different subsystems at different frame-rates on different simulation platforms.
- The slower components are simulated in real-time using a commercial RTOS, often with Simulink support, for faster, cheaper model development.
- Multi-rate also improves performance of non-real-time simulations.
- Multi-rate raises questions of stability and accuracy.

Simulation for Electric Ship Design

- Electric ships pose significant multidisciplinary design problems
- Simulation, including real-time simulation, is an essential technique in tackling these problems
- Different system components and processes require widely varying frame times – from µS to seconds and longer.
- Multi-rate techniques are essential for these simulations
- HSRT techniques are needed in some real-time simulations
- Real-time multi-rate simulation distributed across multiple platforms including HSRT is an attractive approach

Power System for Electric Ship

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Multi-Rate Results

- Multi-Rate Configuration
  - Converter, Switch Controller 2 µsec
  - Feedback Controller 800 µsec
  - Motor/Propeller 50-100 µsec
  - Battery, Ship 1 sec
  - Graphcis 1 sec

- Multi-Rate Performance on 2.16 GHz Mac Running Windows XP
  - All components at 2 µsec: .001x real time
  - Multi-rate, Motor/Propeller 50 µsec 1.2x real-time
  - Multi-rate, Motor/Propeller 100µsec 2.0x real-time

UUV Effects of Multirate Factors

Ship at .1 sec vs .001 sec (Identical Plots)

Current "I3a" to Motor Motor at 2µsec vs 100µsec

Detail of above plot
Real-Time Simulation with FPGA

- FPGA now offers competitive alternative to DSP
- Can be programmed using Simulink FPGA blockset
- Initial tests involved simulation of one converter on a smaller FPGA
- Full 6-pulse model ported to larger FPGA
- Soft processor used for ethernet interface
- FPGA has been interfaced to PC and to external hardware

FPGA Performance vs DSP

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<tr>
<td>6 Pulse BTB - Hammerhead, 23 ODEs</td>
<td>16 µs</td>
<td>AD 21160 DSP</td>
<td>800Mhz</td>
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<tr>
<td>6 Pulse BTB - TigerSharc, 23 ODEs</td>
<td>3.85µs</td>
<td>AD TS101 DSP</td>
<td>250Mhz</td>
</tr>
<tr>
<td>6 Pulse BTB - TigerSharc, 23 ODEs</td>
<td>2.02µs</td>
<td>AD TS201 DSP</td>
<td>500Mhz</td>
</tr>
<tr>
<td>12 Pulse BTB - TigerSharc, 39 ODEs</td>
<td>4.5µs</td>
<td>AD TS201 DSP</td>
<td>500Mhz</td>
</tr>
<tr>
<td>6 Pulse BTB - Xilinx ML-S06, 23 ODEs</td>
<td>320ns</td>
<td>Virtex 5 FPGA</td>
<td>100Mhz</td>
</tr>
</tbody>
</table>

ML506 Board
**Cell Processor Architecture**

- Single Chip Multiprocessor
  - 64-bit Dual-Core PowerPC Main Processor
  - 8 Single-Instruction, Multiple-Data (SIMD) Vector Processor Cores
  - Shared Memory with Asynchronous DMA

**Cell Processor Features**

**Cell Processor Issues**

- Development Board Availability
  - Limited number of suppliers/configurations

- Development Tools
  - Very young tools, not fully evolved yet

- Performance
  - Graphic/Entertainment processing emphasis – Does this really translate to executing models?
  - Emphasis on throughput – Is latency an issue?

**Vendor Data For Cell Processor Performance**

- Performance relative to single processor (relative to 1)
- In all cases, results are normalized to single processor, which reflects the theoretical capabilities of the single processor and other processors.
Conclusions

- Modern technologies can support real-time simulations with frame times in hundreds of nanoseconds
- Combining high-speed processors and RT-Linux systems provides real-time multi-rate simulations with high-speed components
- FPGA is the current processor of choice for high-speed components
- Cell architecture may provide a more convenient high-speed processor
- New software tools are needed to support high-speed multi-rate real-time simulation
- Further research is needed in several areas

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Questions?